Design, Fabrication and Characterization of a Radiation Hardened SONOS-CMOS 1-4Mb EEPROM for Space and Military Systems*

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We present the design, fabrication and characterization of a radiation-hardened, SONOS-CMOS 1-4 Mb EEPROM for space and military systems. The 1 Mb design employs a 2T memory cell design (one NMOS transistor for read access and one SONOS memory transistor) with 128K byte page (128K x 8) architecture. Sensing is accomplished with a comparison of the SONOS memory transistor current level to the average current level of two SONOS reference transistors, which are erase/programmed at the same time as the memory transistors in the array. An on-chip, charge-pump provides a variable negative voltage to obtain a programming voltage of $V_{DD} - V_P = 7V$, where V_{DD} is 3.3 or 5V. In high radiation environments, the charge-pump can be disabled. The array operates with 2.5ms write, 7.5ms clear and a read access time less than 250 ns. The array exceeds 10 year retention over a temperature range of –55 to +125C with an endurance of 1E5 write cycles and tolerates total dose radiation in excess of 300Krad (Si) and transient radiation greater than 1E8 Rad(Si)/s and NV Data Upset greater than 1E12 Rad(Si)/s. SEU Immunity is in excess of 35 MeV/mg/cm^2 for program and 60 MeV/mg/cm^2 for read operation. There is no permanent data loss mechanism in the SONOS transistor up to LET's over 90 MeV-/mg/cm^2. An advanced 0.35micron, 4-level tungsten plug, CMP, high-density interconnect SONOS/CMOS technology will be described for 4Mb SONOS-CMOS EEPROMs. SONOS-CMOS radiation-hardened EEPROMs are flight-qualified and currently employed in advanced space-borne and military systems.

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*Work supported by Clyde Elliott of the US Army Space and Defense Missile Command (USASMDC) and monitored by Jim Sheehy and Gary Grant of the ATK Mission Research Center in Huntsville, Ala.